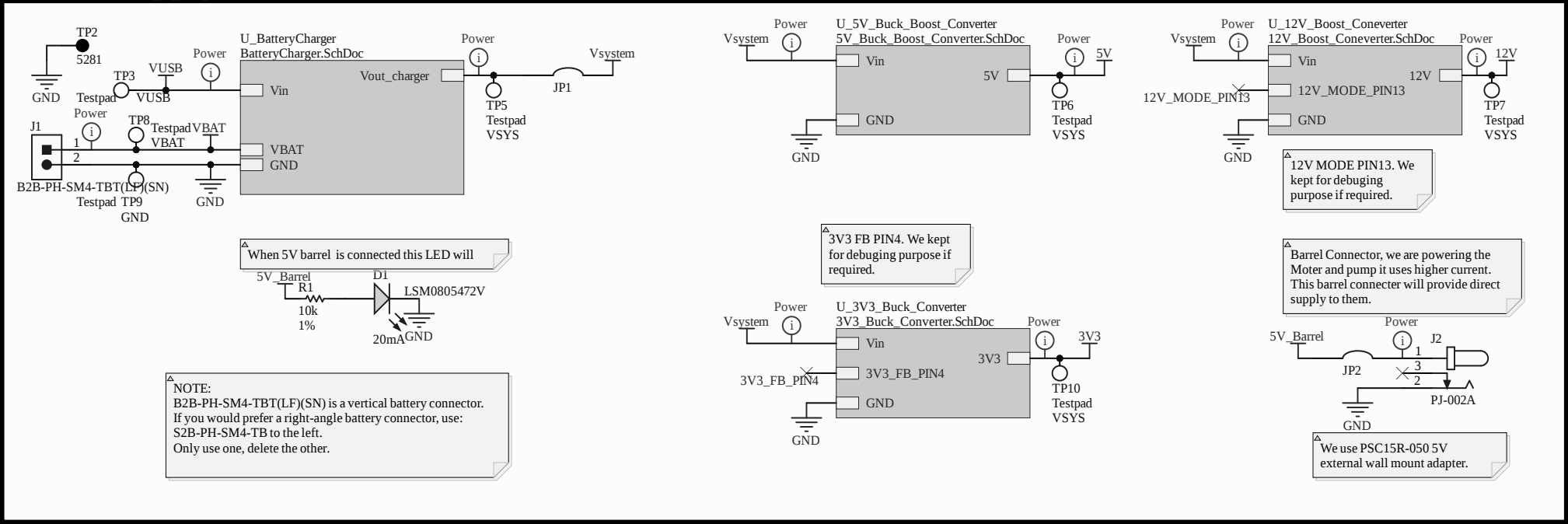


Power Supply



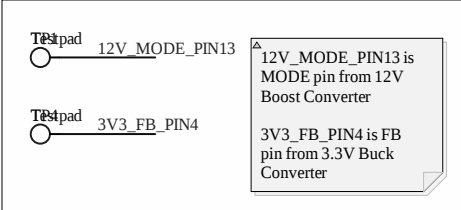
Notes

Section to add version notes or any other general information

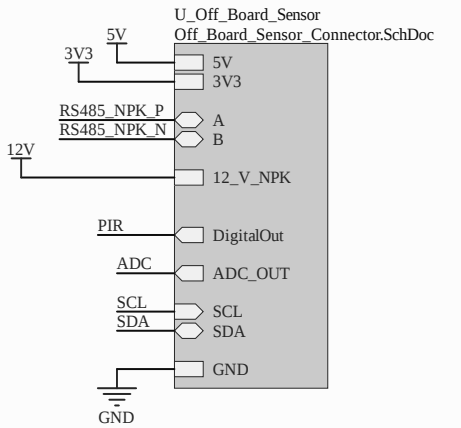
Add your power architecture here!

Don't forget:
0R jumpers in series with your power lines
1x through hole test point per power net

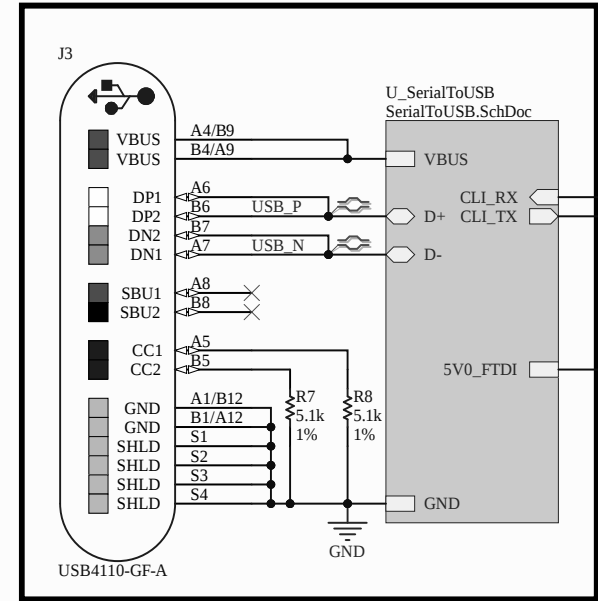
Test Points + Fiducials



Off Board Sensors

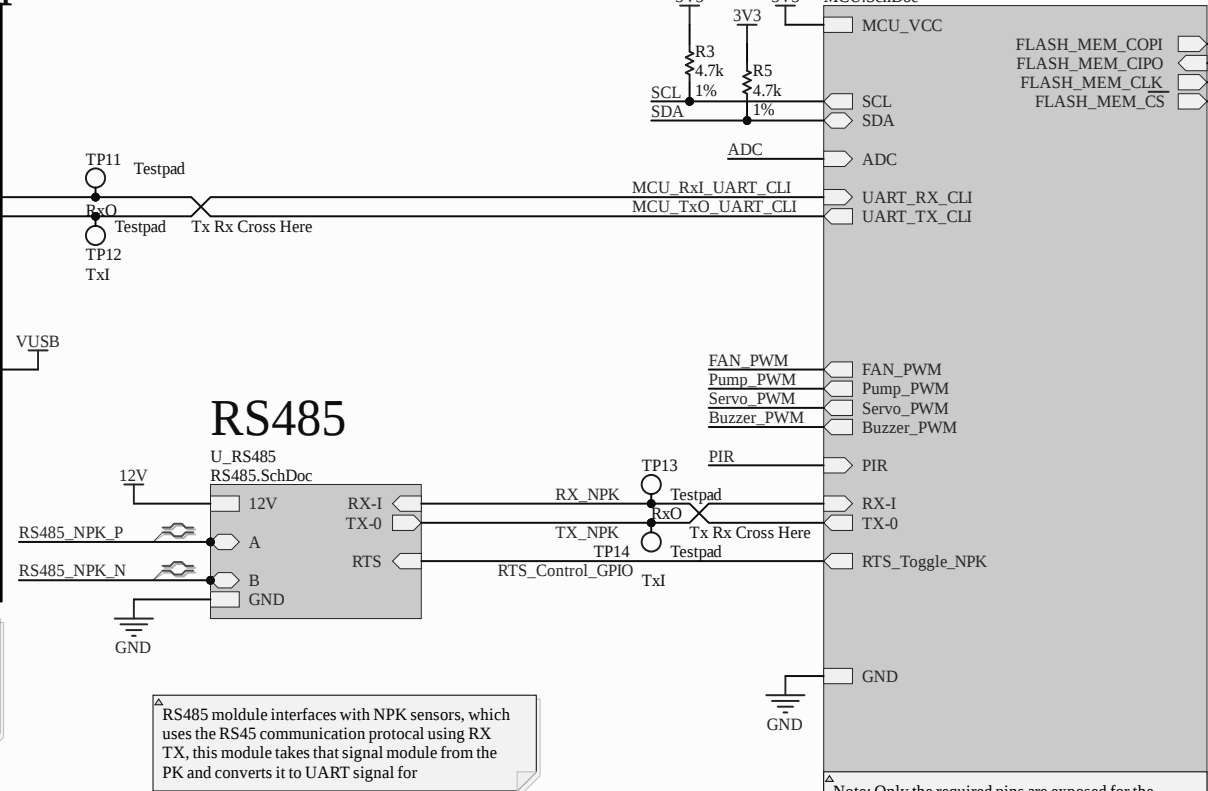


USB C Connector + FTDI Chip

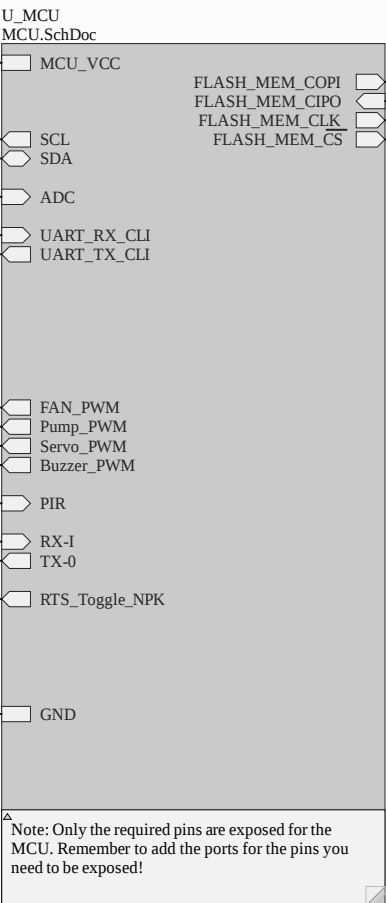


NOTE:
The FTDI Chip is a useful chip that allows us to convert USART messages into USB signals. It allows us to connect the MCU directly to the USB port of a computer and use the serial terminal (it is similar to the bridge used on the SAMW25 Xplained Board). The FTDI device also contains protection circuitry for the USB.

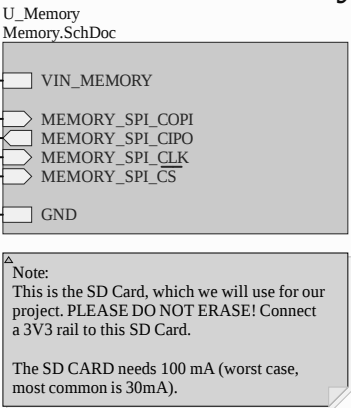
RS485



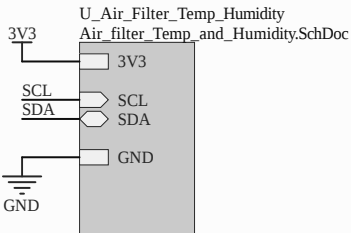
Microcontroller



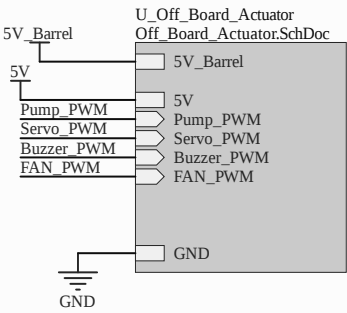
SD Card Memory

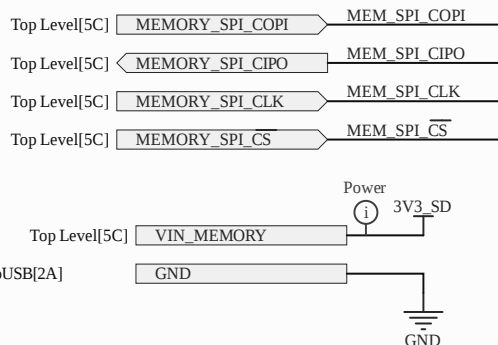


I2C sensors

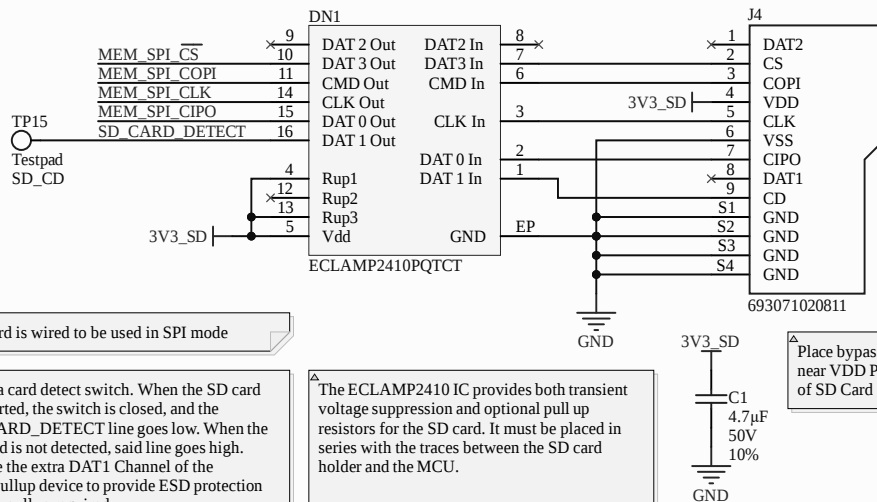


Actuators





SD CARD

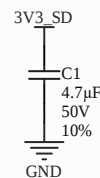


SD Card is wired to be used in SPI mode

CD is a card detect switch. When the SD card is inserted, the switch is closed, and the SD_CARD_DETECT line goes low. When the SD card is not detected, said line goes high. We use the extra DAT1 Channel of the ESD/Pullup device to provide ESD protection and the pullup required.

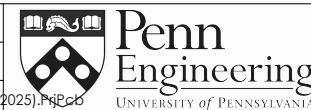
Use of card detect is optional, but is provided if you want to use it.

The ECLAMP2410 IC provides both transient voltage suppression and optional pull up resistors for the SD card. It must be placed in series with the traces between the SD card holder and the MCU.

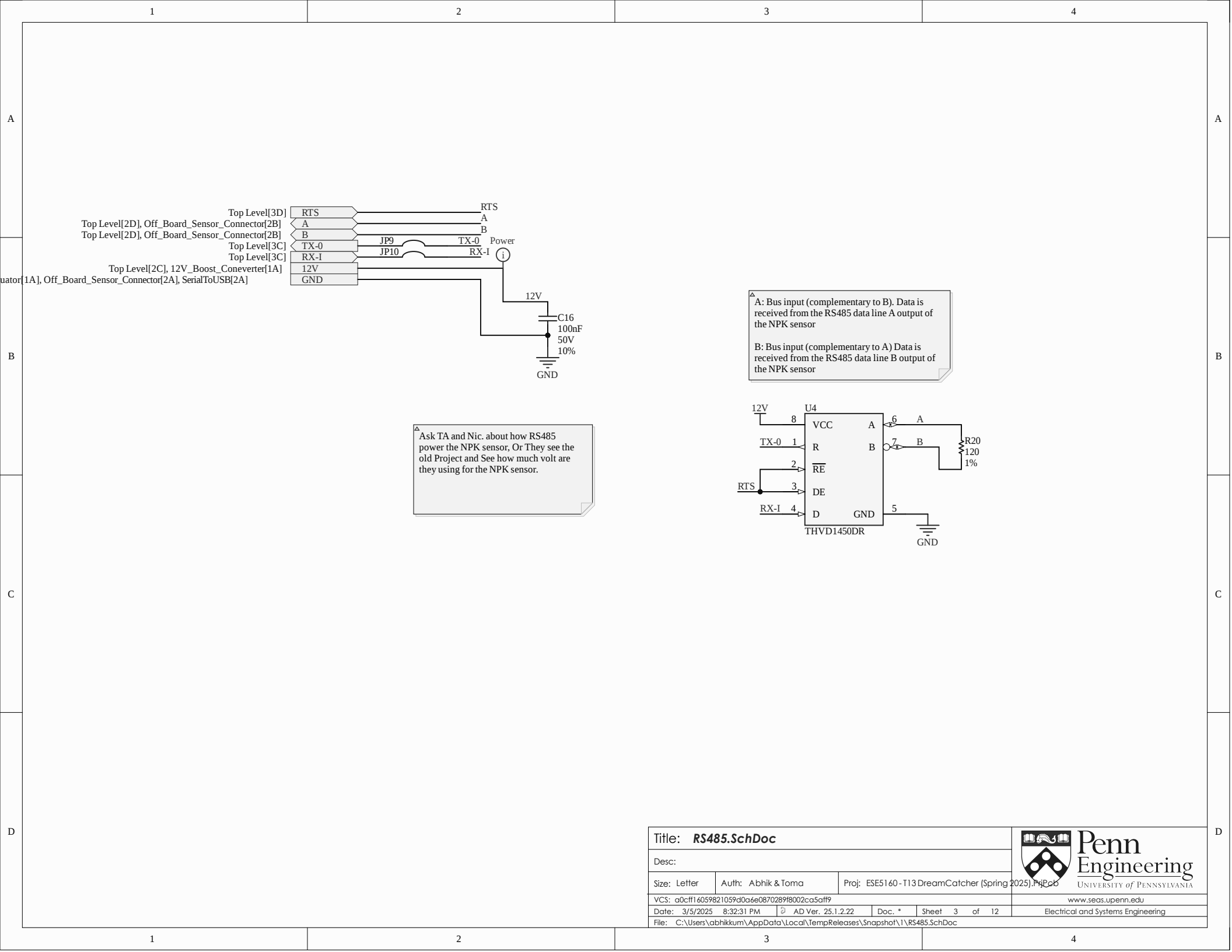


Place bypass near VDD Pin of SD Card

Title: Memory.SchDoc				 Penn Engineering UNIVERSITY OF PENNSYLVANIA
Desc: SD Card				
Size: Letter	Auth: Abhik & Toma	Proj: ESE5160-T13 DreamCatcher (Spring 2025), PCB		
VCS: a0cff16059821059d0a6e0870289f8002ca5aff9				www.seas.upenn.edu
Date: 3/5/2025 8:32:31 PM	AD Ver. 25.1.2.22	Doc. *	Sheet 2 of 12	Electrical and Systems Engineering
File: C:\Users\abhik\AppData\Local\Temp\Releases\Snapshot\1\Memory.SchDoc				



www.seas.upenn.edu
Electrical and Systems Engineering



Title: **RS485.SchDoc**

Desc:

Size: Letter

Auth: Abhik & Toma

Proj: ESE5160 - T13 DreamCatcher (Spring 2025), P6 PCB

VCS: a0cff16059821059d0a6e0870289f8002ca5aff9

Date: 3/5/2025 8:32:31 PM

AD Ver. 25.1.2.22

Doc. *

Sheet 3 of 12

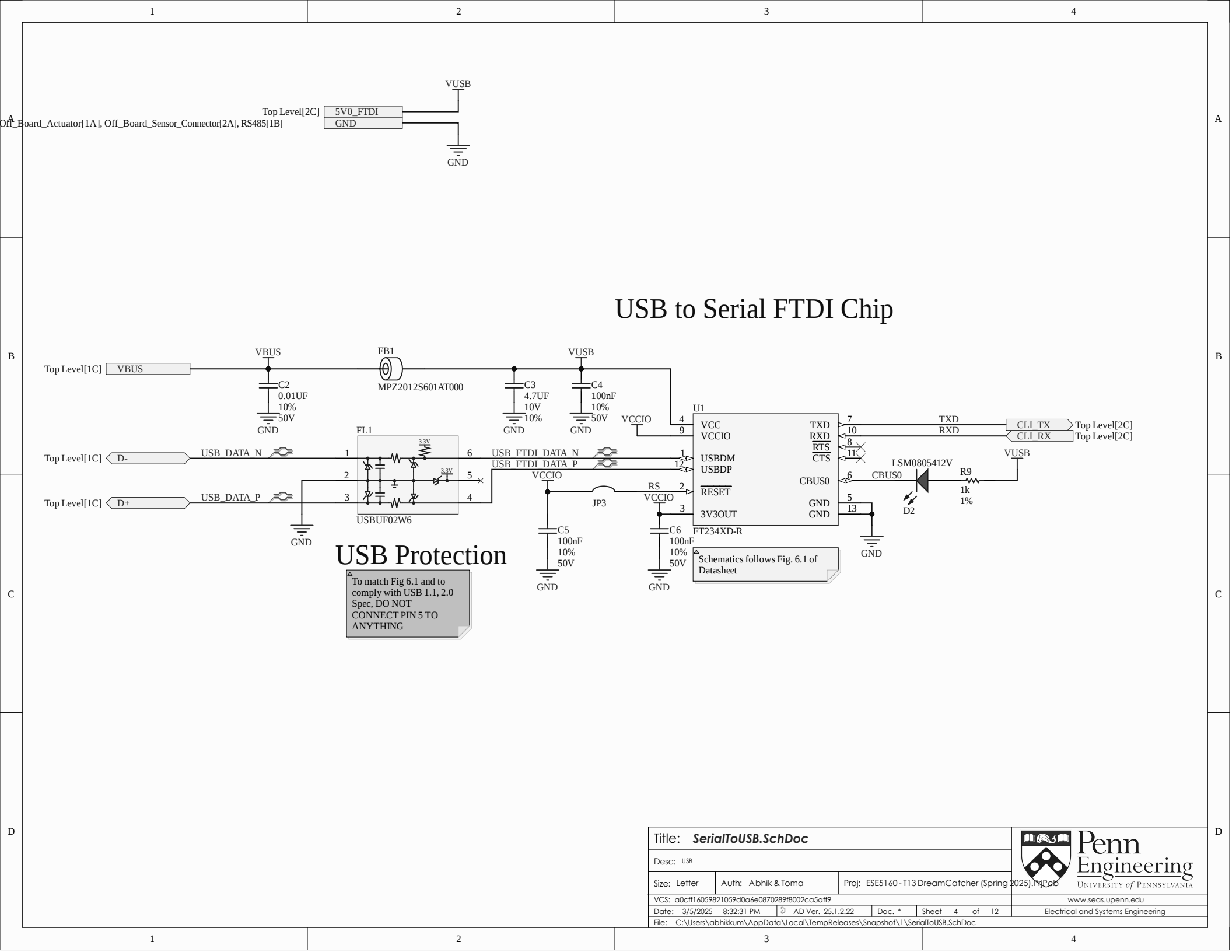
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Title: **SerialToUSB.SchDoc**

Desc: USB

Size: Letter

Auth: Abhik & Toma

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Date: 3/5/2025 8:32:31 PM

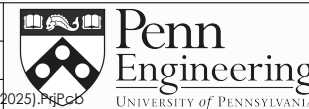
AD Ver. 25.1.2.22

Doc. *

Sheet

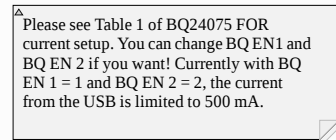
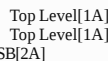
4 of 12

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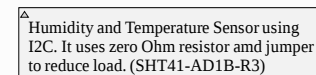
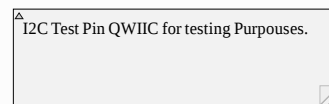


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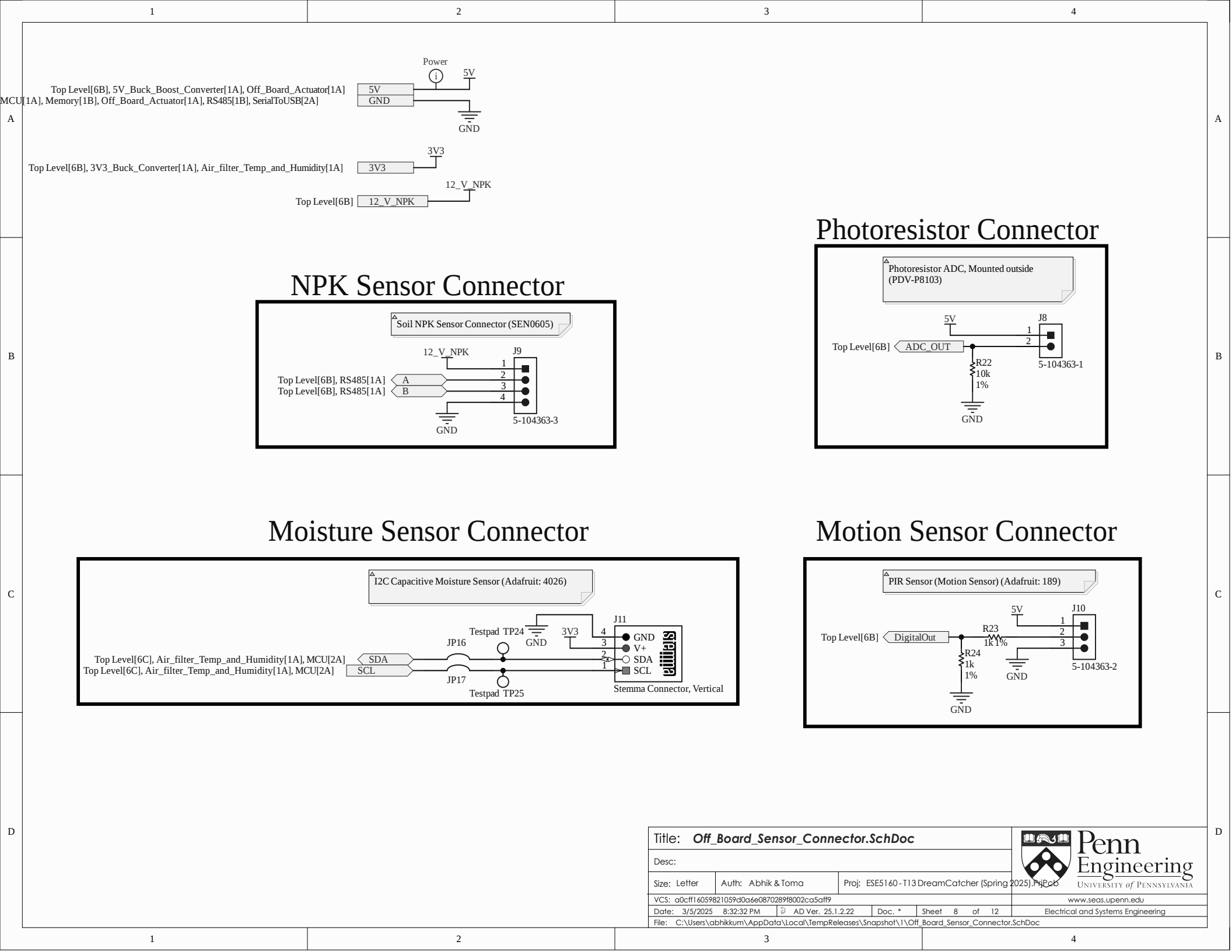


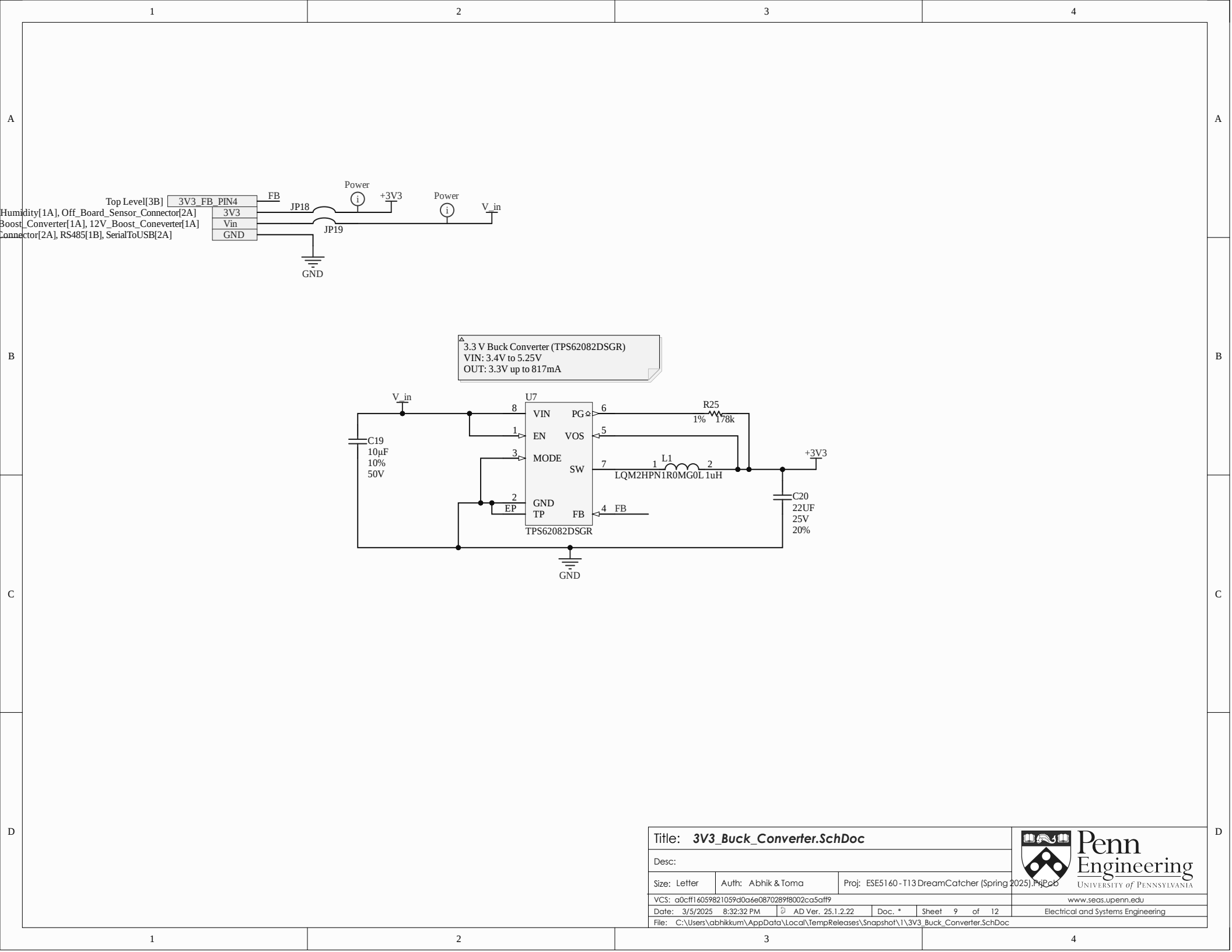
Air Quality Sensor

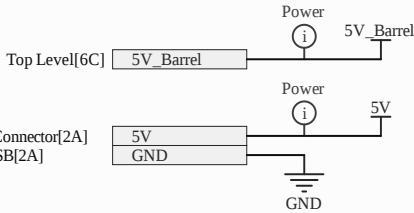


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Date: 3/5/2025 8:32:32 PM			Ad Ver. 25.1.2.22		Doc. *	Sheet 7 of 12	Electrical and Systems Engineering
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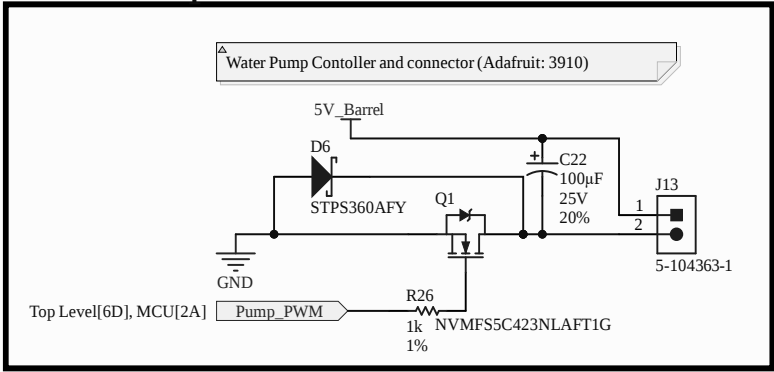




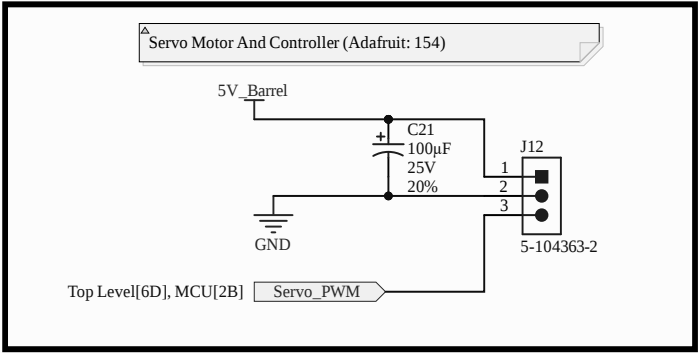




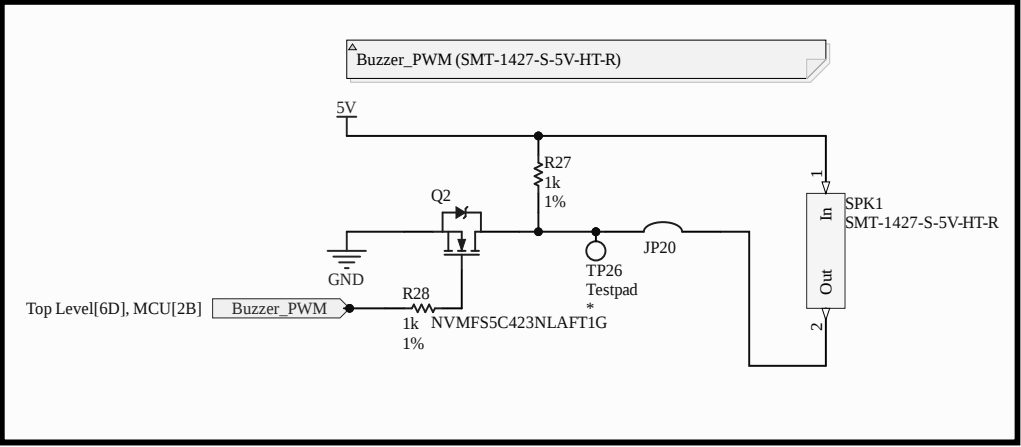
Water Pump Controller and Connector



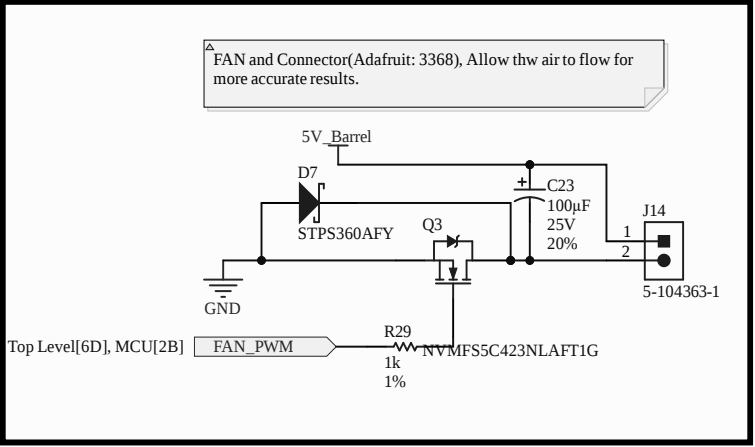
Servo Motor and Controller

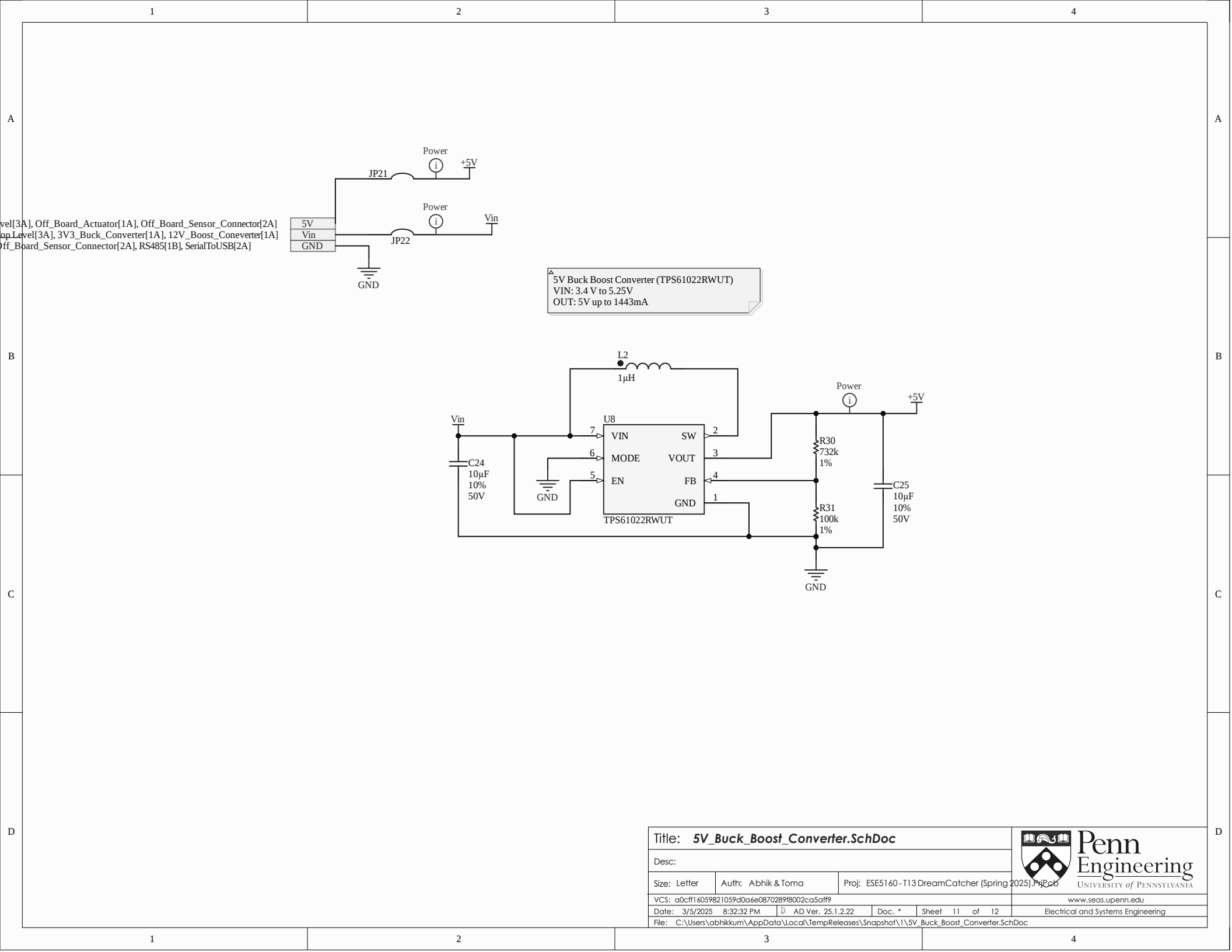


Buzzer



Fan and Connector





Title: 5V_Buck_Boost_Converter.SchDoc

Desc:

Size: Letter

Auth: Abhik & Toma

Proj: ESE5160-T13 DreamCatcher (Spring 2025), PCB

VCS: a0cff16059821059d0a6e0870289f8002ca5aff9

Date: 3/5/2025 8:32:32 PM

AD Ver. 25.1.2.22

Doc. *

Sheet 11 of 12

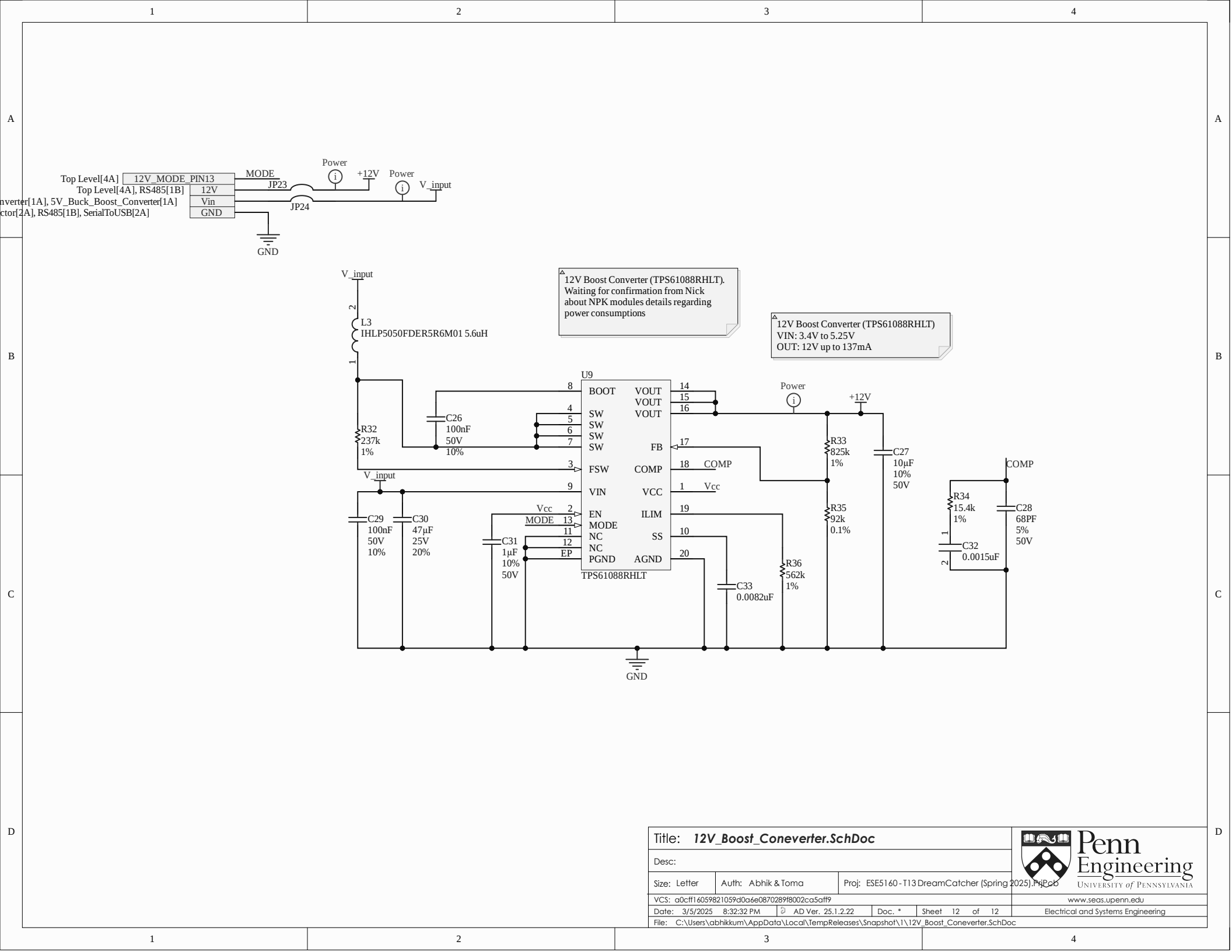
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File: C:\Users\abhik\AppData\Local\Temp\Releases\Snapshot\1\5V_Buck_Boost_Converter.SchDoc



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Title: 12V_Boost_Coneverter.SchDoc

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Size: Letter

Auth: Abhik & Toma

Proj: ESE5160 - T13 DreamCatcher (Spring 2025), PnP

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Date: 3/5/2025 8:32:32 PM

AD Ver. 25.1.2.22

Doc. *

Sheet 12 of 12

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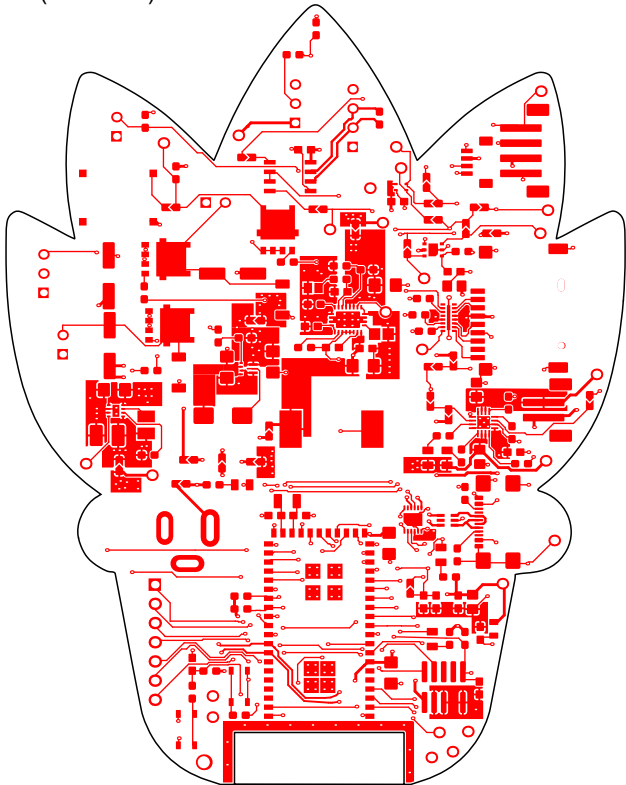
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L1 (Scale 1:1)



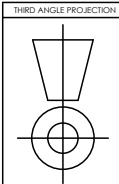
Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.03mm(1.00mil)	PSR-4000BN DI Colors	Solder Mask	GTS
Nickel, Gold	Top Surface Finish	0.00mm(0.16mil)		Surface Finish	
Copper	L1	0.04mm(1.38mil)		Signal	GTL
Core		0.20mm(7.96mil)	FR408HR 2113	Dielectric	
Copper	L2 (GND)	0.02mm(0.69mil)		Signal	G1
		0.99mm(39.00mil)	FR408HR	Dielectric	
Copper	L3 (Power)	0.02mm(0.69mil)		Signal	G2
Core		0.20mm(7.96mil)	FR408HR 2113	Dielectric	
Copper	L4	0.04mm(1.38mil)		Signal	GBL
Nickel, Gold	Bottom Surface Finish	0.00mm(0.16mil)		Surface Finish	
Surface Material	Board Layer Stack Bottom Solder	0.03mm(1.00mil)	PSR-4000BN DI Colors	Solder Mask	GBS
	Board Layer Stack Bottom Overlay			Legend	GBO
Total thickness: 1.56mm(61.37mil)					

Manufacturing Notes:

- 1
- All layers are unmirrored - you should be able to "see straight through."
- 2
- Controlled Dielectric: NO
- 3
- Controlled Impedance: NO
- 4
- Thickness tolerance +/-10%
- 5
- UL Marking Required: NO
- 6
- RoHS Marking: NO
- 7
- ITAR: NO

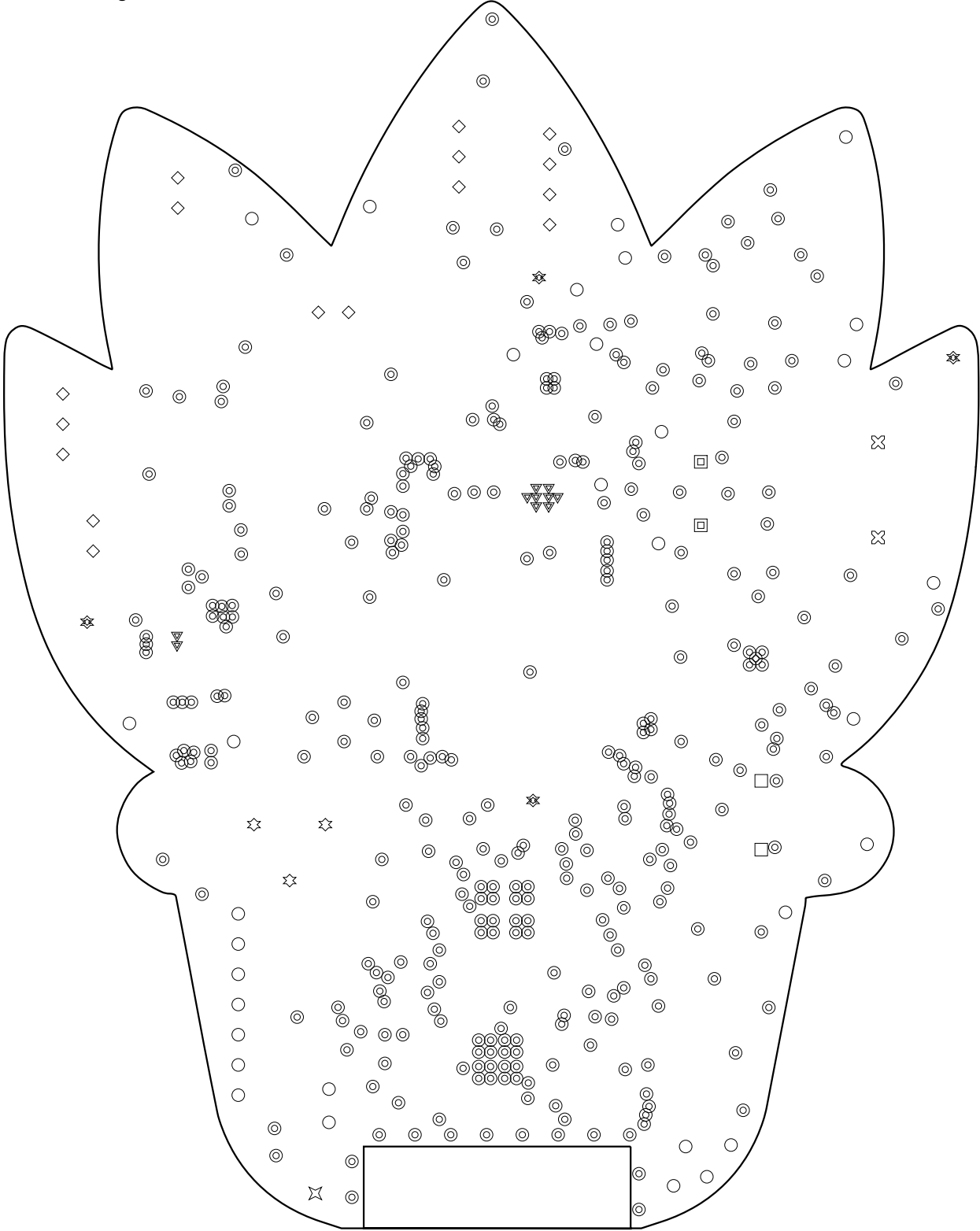
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		DWG NO:	
		SCALE:	
		FILE NAME: FabricationDrawings.PCBDwf	
		SHEET: 1 OF 12	



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Drill Drawing View



REV STATUS OF SHEETS	REV SHEET	DWG NO: =DOC_NO_ASSY_DWG										ZONE	REV	REVISIONS		
														DESCRIPTION	DATE	APPROVED

Drill Table

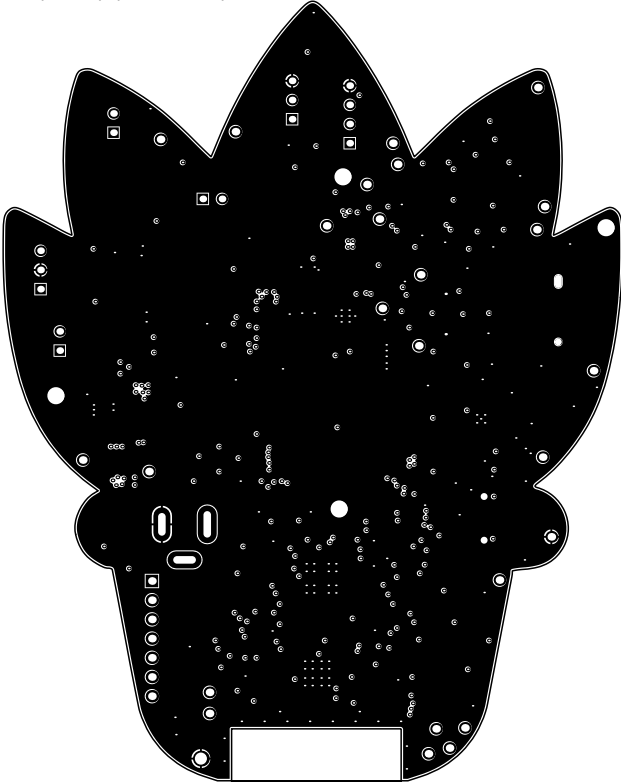
Symbol	Count	Hole Size	Plated	Hole Tolerance
✱	4	2.00mm(78.74mil)	Non-Plated	
○	32	1.02mm(40.00mil)	Plated	
☆	3	1.00mm(39.37mil)	Plated	
◇	16	0.89mm(35.04mil)	Plated	
⊠	2	0.90mm(35.43mil)	Non-Plated	
□	2	0.65mm(25.59mil)	Non-Plated	
✧	1	1.60mm(62.99mil)	Plated	
◎	339	0.20mm(8.00mil)	Plated	
▼	10	0.20mm(7.87mil)	Plated	
▣	2	0.32mm(12.50mil)	Plated	

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DESIGNER: =PCB_DESIGNER		=PCB_DESIGNER		=PCB_DESIGNER					
CHECKER: =PCB_CHECKER		=PCB_CHECKER		=PCB_CHECKER					
Reference Documents		BOM DOC: =DOC_NO_BOM		ASSY DOC: =DOC_NO_FAB_DWG		DESIGN ITEM: SRC-ESE5160 - T13	DESIGN ITEM REVISION: A.4		
SCH DOC: =DOC_NO_SCH_DWG		PCB DOC: =PCB_DWG_NO		TITLE: =PCB_TITLE_1 =PCB_TITLE_2		SIZE: B	CAGE CODE: =CAGE_CO	DWG NO:	REV: A.
NEXT ASSY		USED ON		APPLICATION		SCALE:		FILE NAME: FabricationDrawings.PCBDwf	SHEET: 2 OF 12

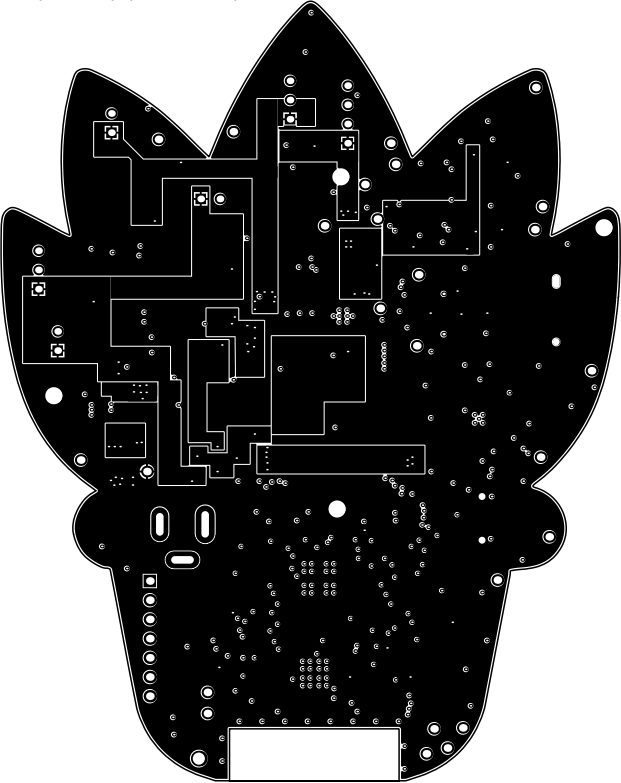
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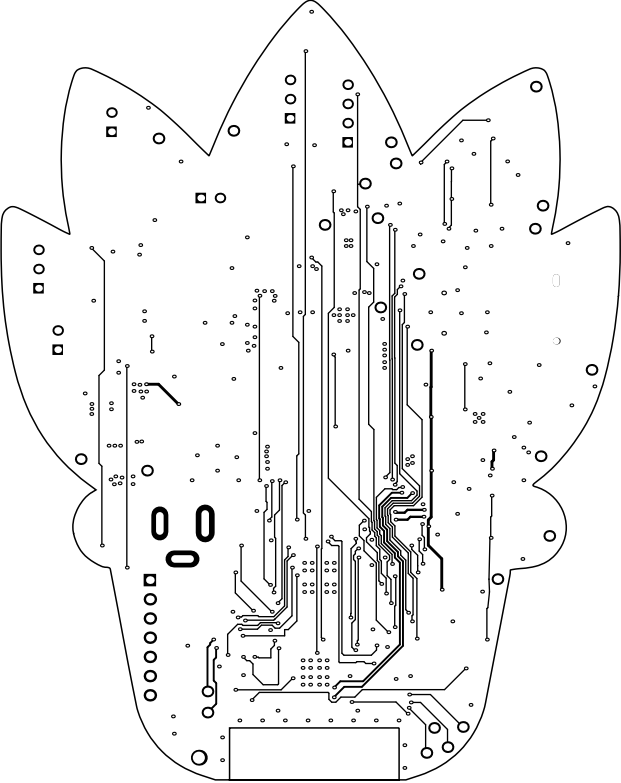
L2 (GND) (Scale 1:1)



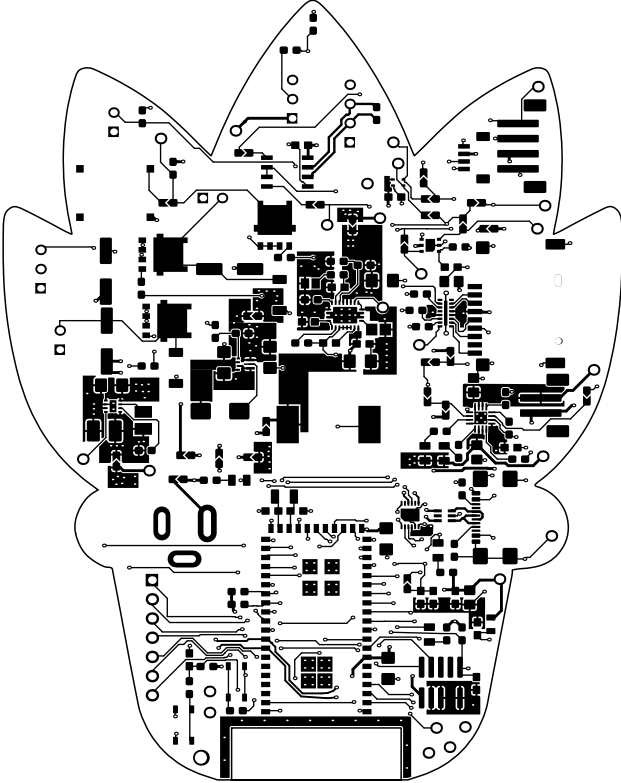
L3 (Power) (Scale 1:1)



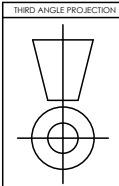
L4 (Scale 1:1)



L1 (Scale 1:1)



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Reference Documents					DESIGN ITEM: SRC-ESE5160 - T13	
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					SHEET: 3 OF 12	

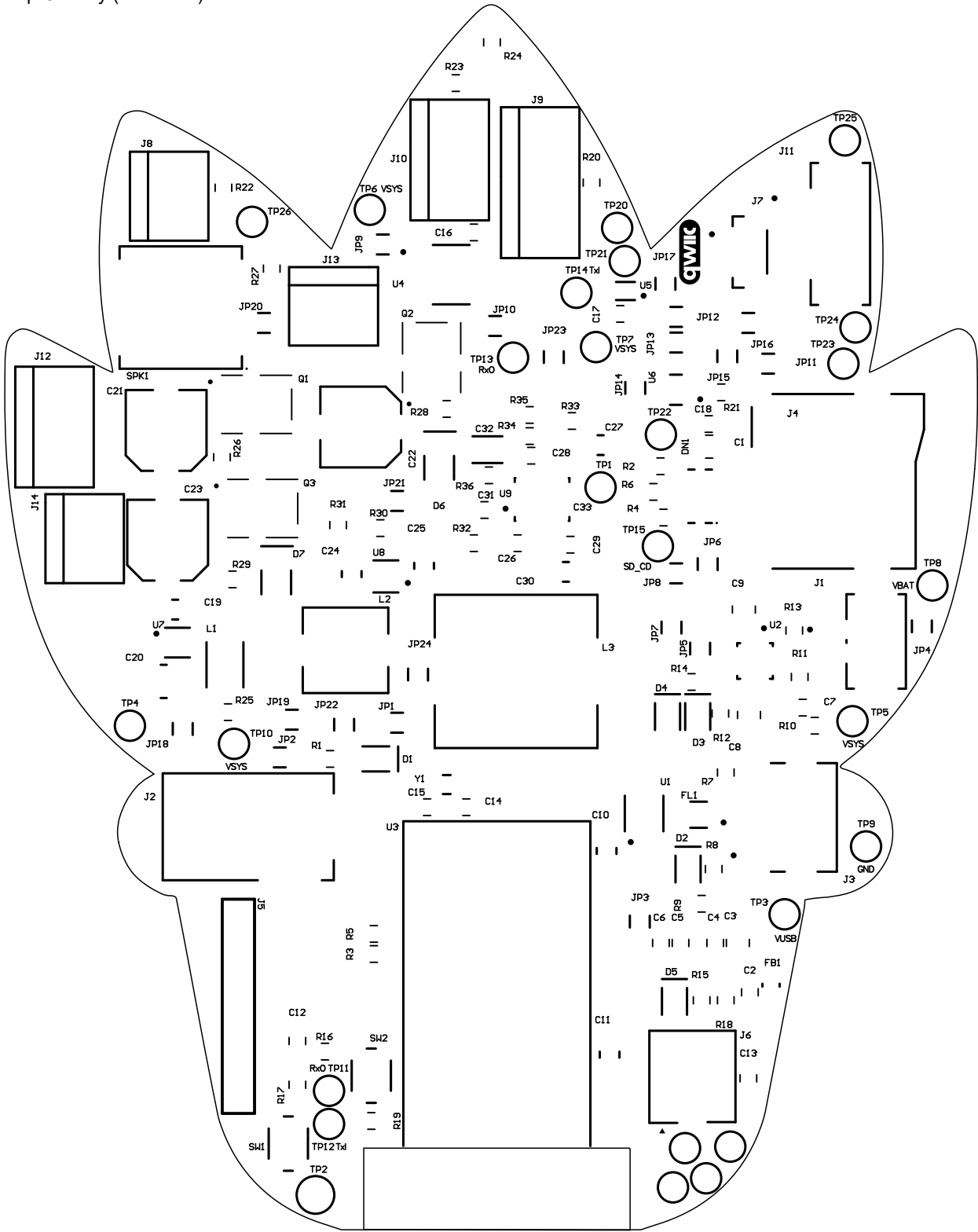


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REV: A.4

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Top Overlay (Scale 2:1)



REV STATUS OF SHEETS	REV										REVISIONS				
	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED

APPROVALS

DATE

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DESIGN ITEM REVISION: A.4

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SIZE: B

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SCALE:

FILE NAME: FabricationDrawings.PCBDwf

SHEET: 4 OF 12

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APPROVALS

DATE

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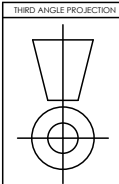
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REV: A.

SCALE:

FILE NAME: FabricationDrawings.PCBDwf

SHEET: 4 OF 12

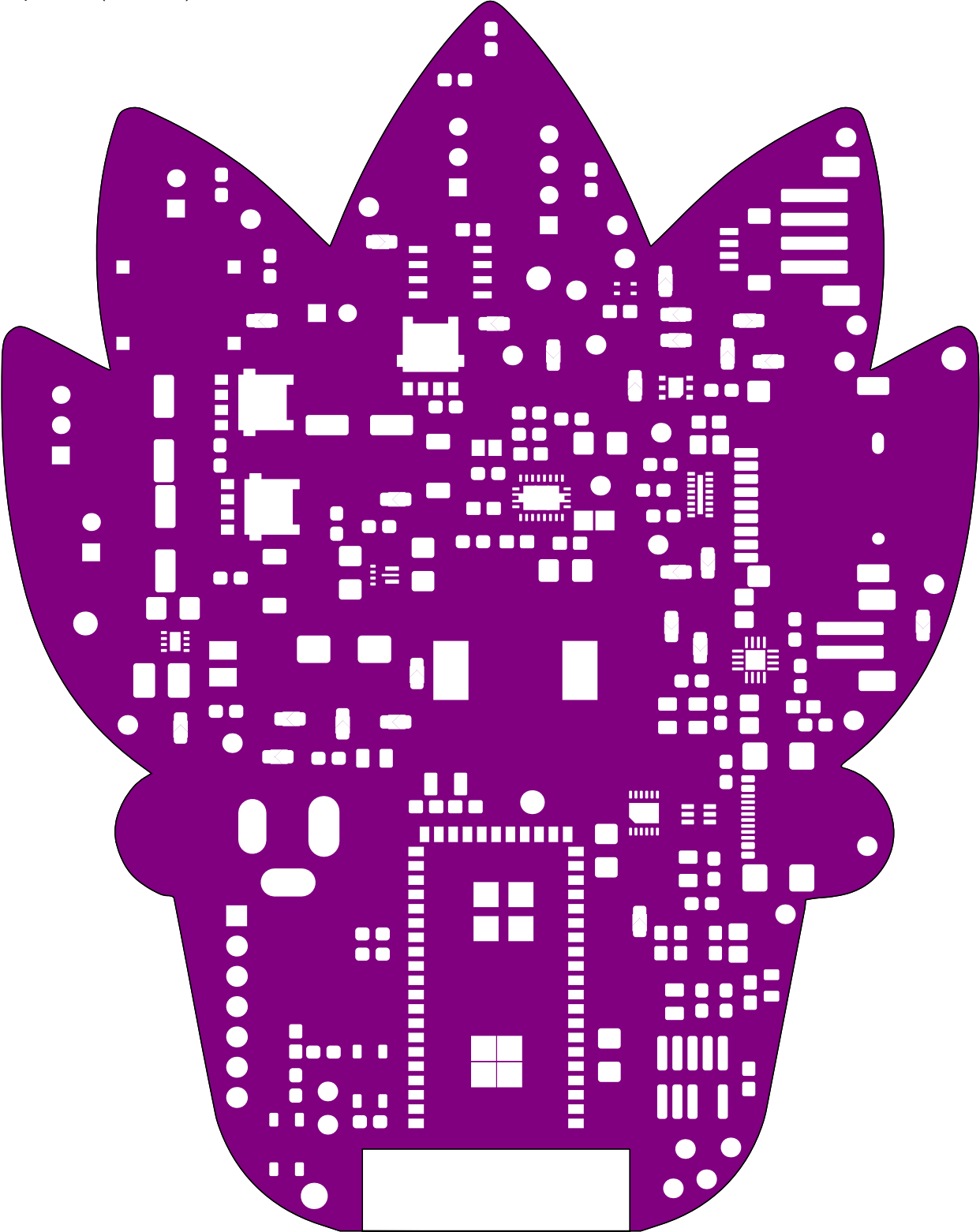


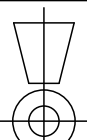
APPLICATION

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	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED

Top Solder (Scale 2:1)

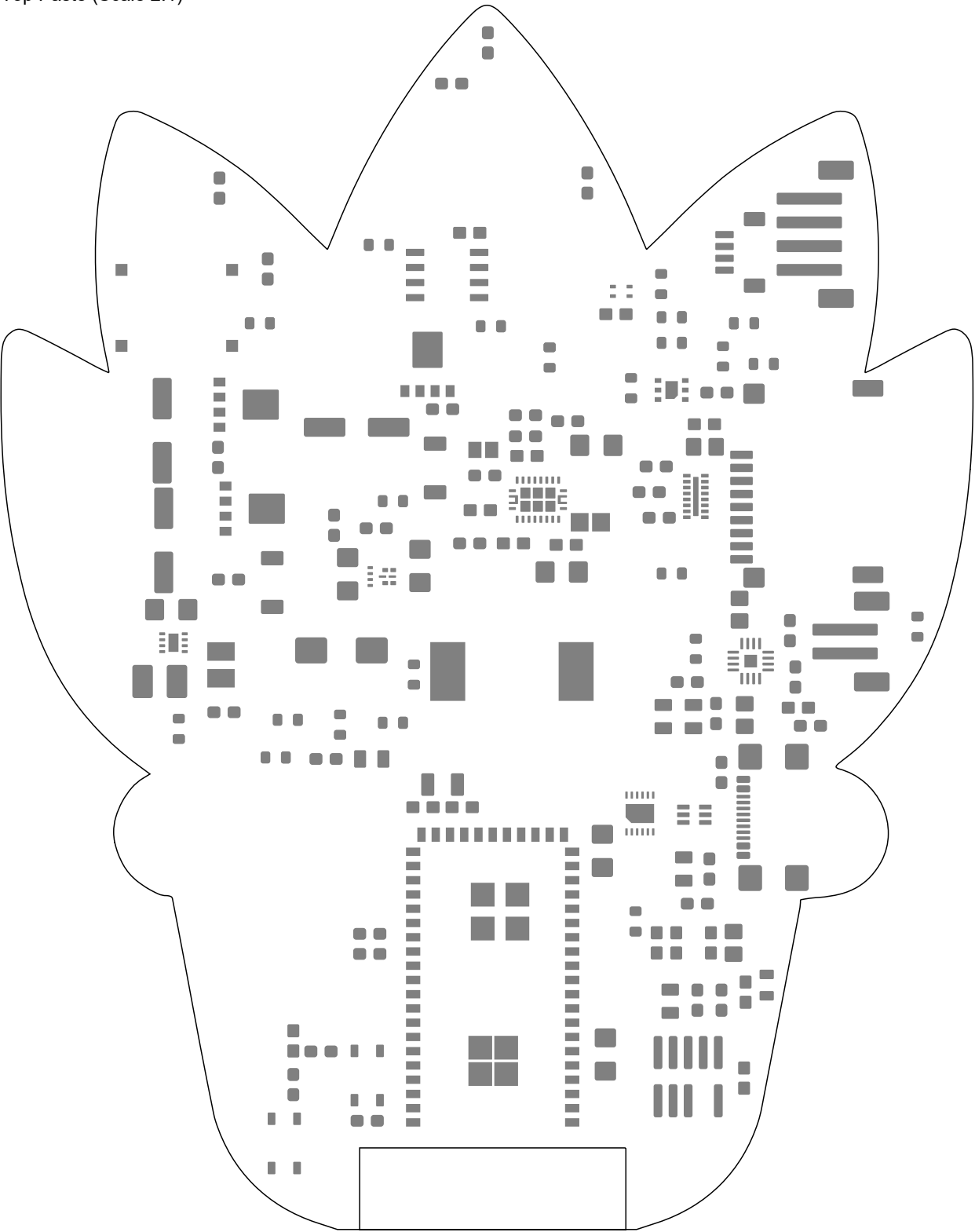


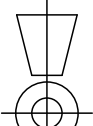
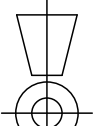
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										REV:	
				SCALE:		FILE NAME: FabricationDrawings.PCBDwf		SHEET: 5 OF 12			

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[illegible]

Top Paste (Scale 2:1)



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NEXT ASSY		USED ON		SCALE:		FILE NAME: FabricationDrawings.PCBDwf		SHEET: 6 OF 12	
APPLICATION									

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REV STATUS OF SHEETS	REV											REVISIONS				
	SHEET											ZONE	REV	DESCRIPTION	DATE	APPROVED

L1 (Scale 2:1)



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DESIGNER: =PCB_DESIGNER		=PCB_DESIGNER		=Address3					
CHECKER: =PCB_CHECKER		=PCB_CHECKER		=Address4					
Reference Documents		BOM DOC: =DOC_NO_BOM		ASSY DOC: =DOC_NO_FAB_DWG		SCH DOC: =DOC_NO_SCH_DWG		PCB DOC: =PCB_DWG_NO	
THIRD ANGLE PROJECTION		NEXT ASSY		USED ON		APPLICATION		DESIGN ITEM: SRC-ESE5160 - T13	
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								SHEET: 7 OF 12	

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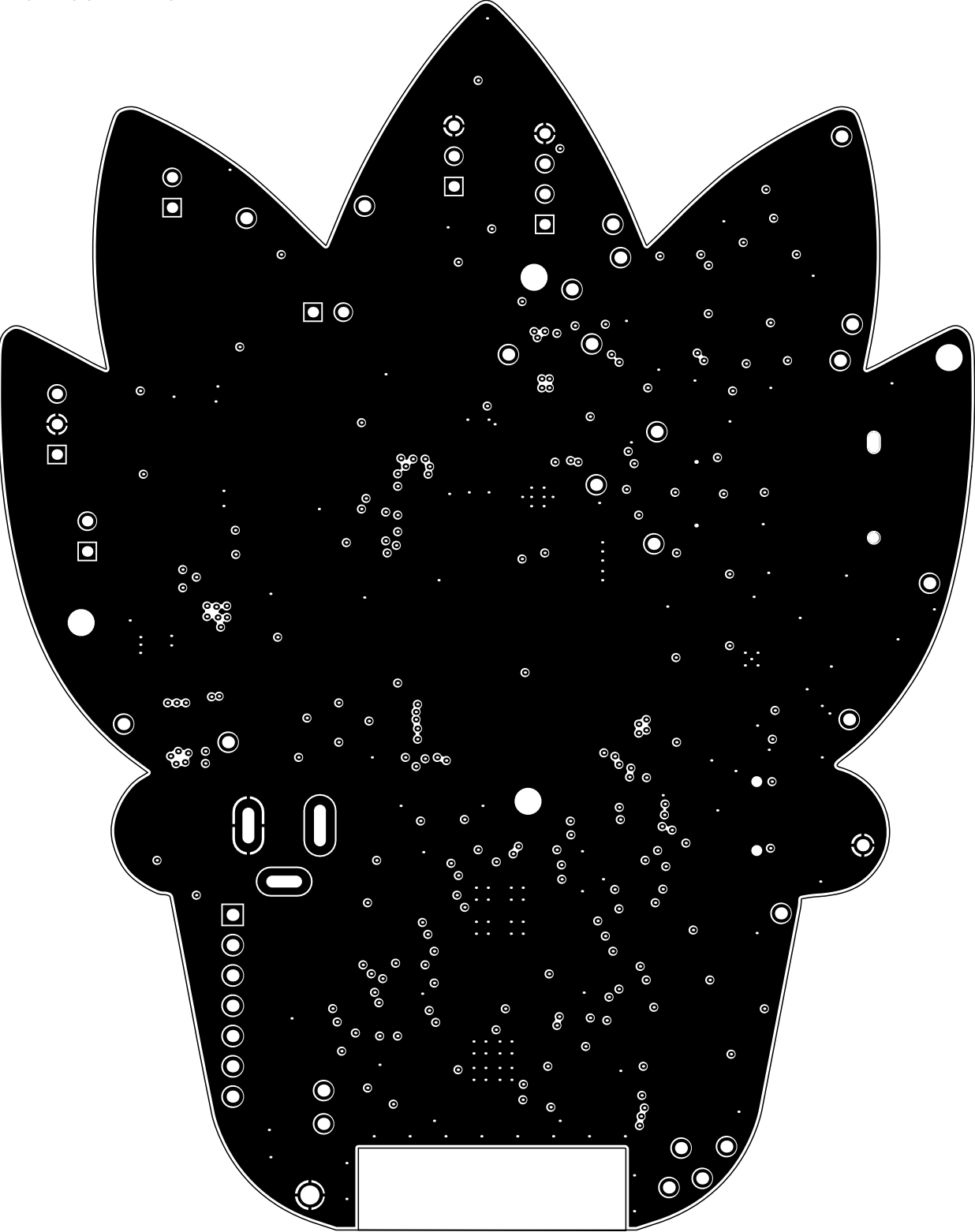
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REV STATUS OF SHEETS	REV										REVISIONS				
	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED

L2 (GND) (Scale 2:1)

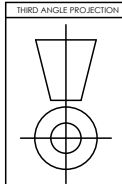
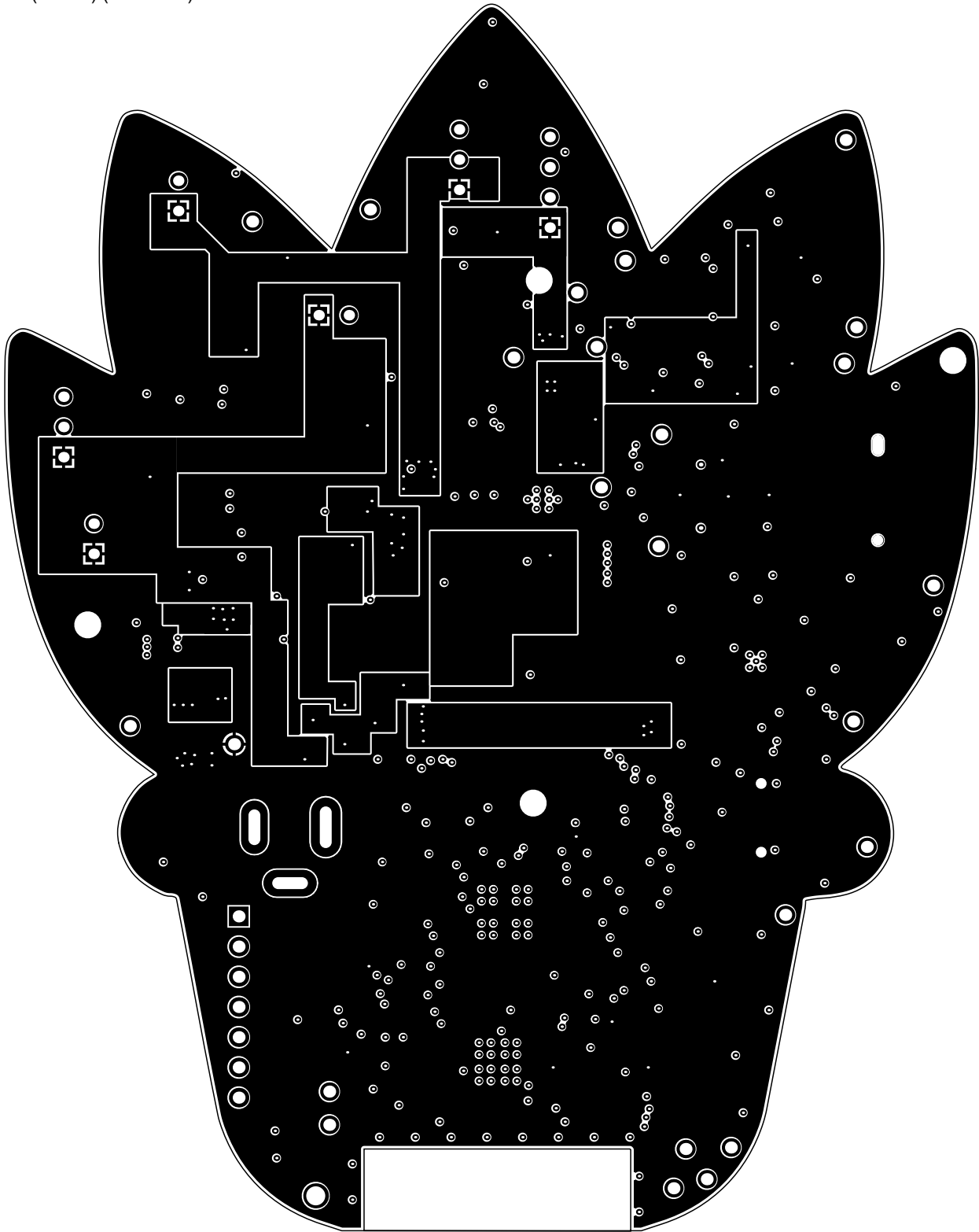


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NEXT ASSY		USED ON		SCALE:		FILE NAME: FabricationDrawings.PCBDwf		SHEET: 8 OF 12	
APPLICATION									

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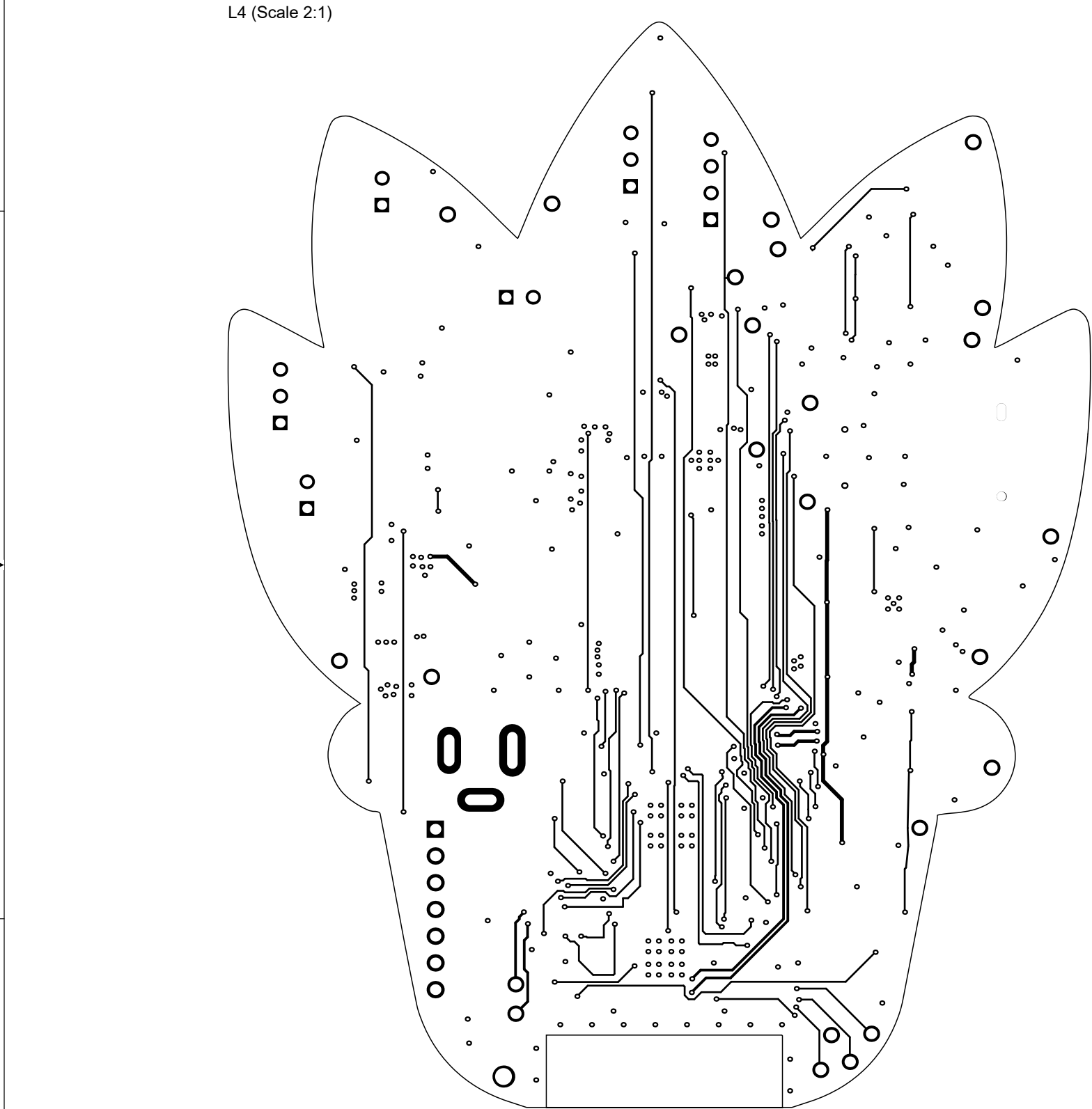
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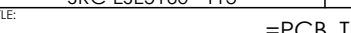


APPLICATION	
NEXT ASSY	USED ON

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Reference Documents					
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SCALE:		FILE NAME: FabricationDrawings.PCBDwf		SHEET: 9 OF 12	

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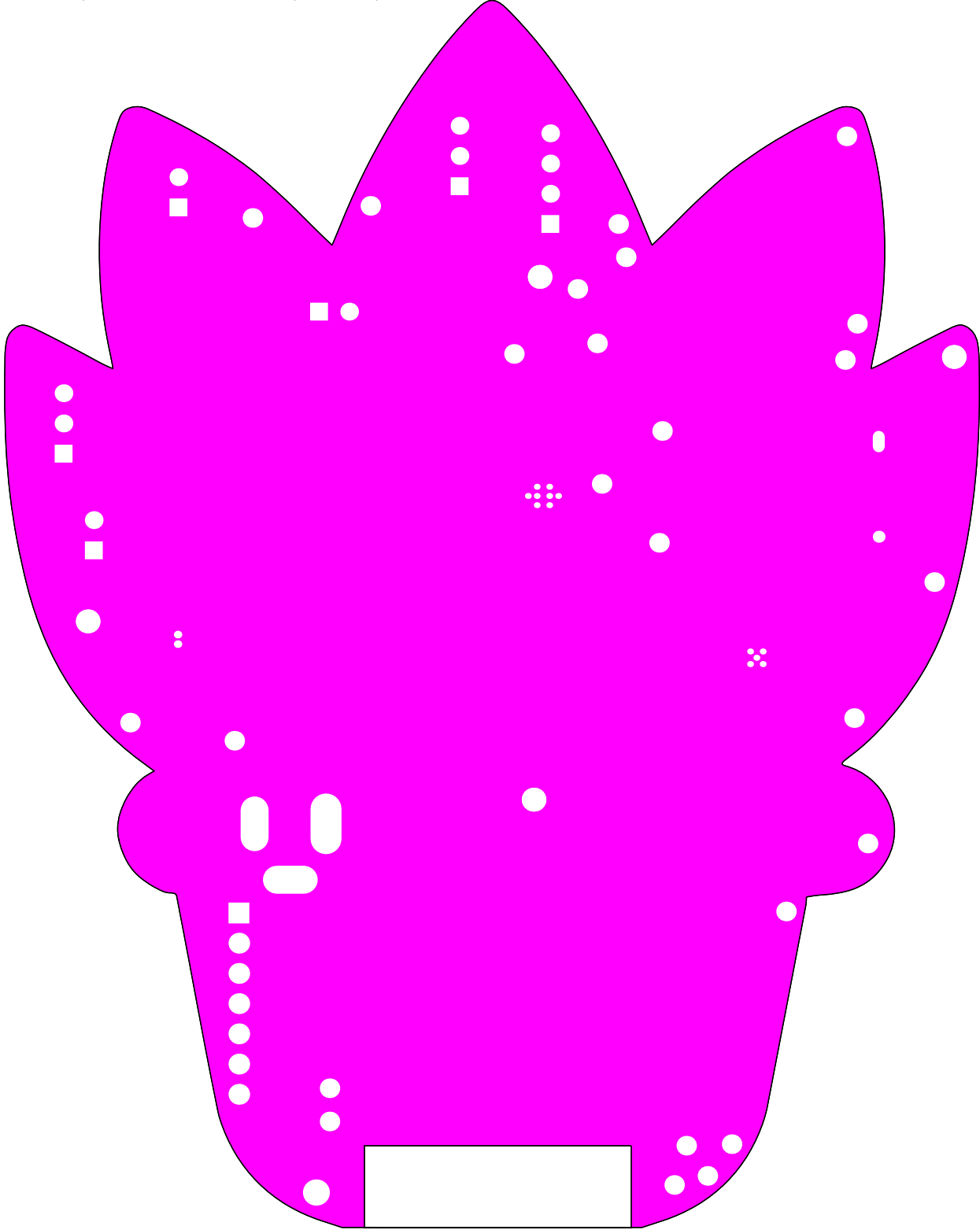
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NEXT ASSY		USED ON		SCALE:		FILE NAME: FabricationDrawings.PCBDwf		SHEET: 10 OF 12	
APPLICATION									

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[illegible]

Board Layer Stack Bottom Solder (Scale 2:1)

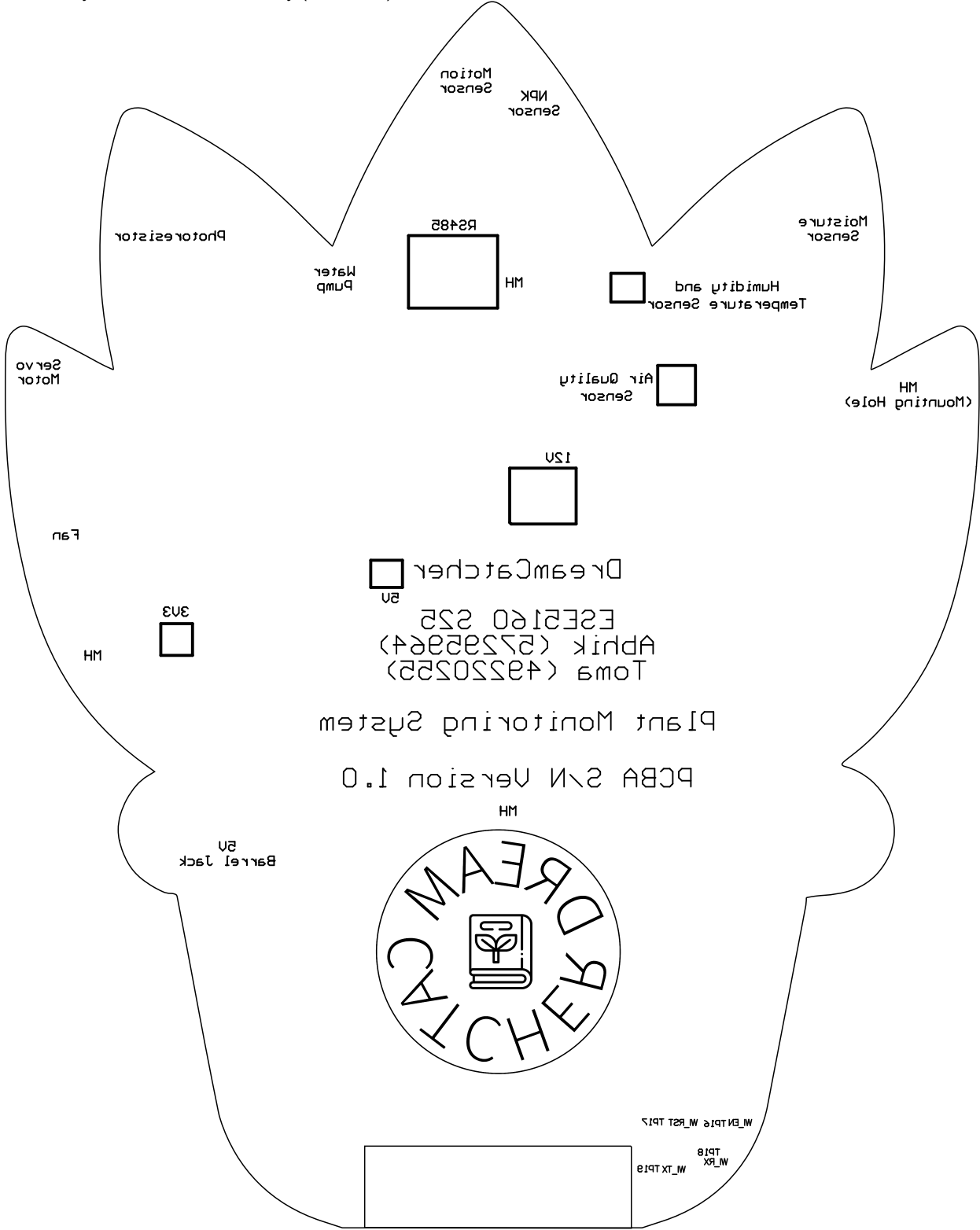


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NEXT ASSY		USED ON									
APPLICATION											

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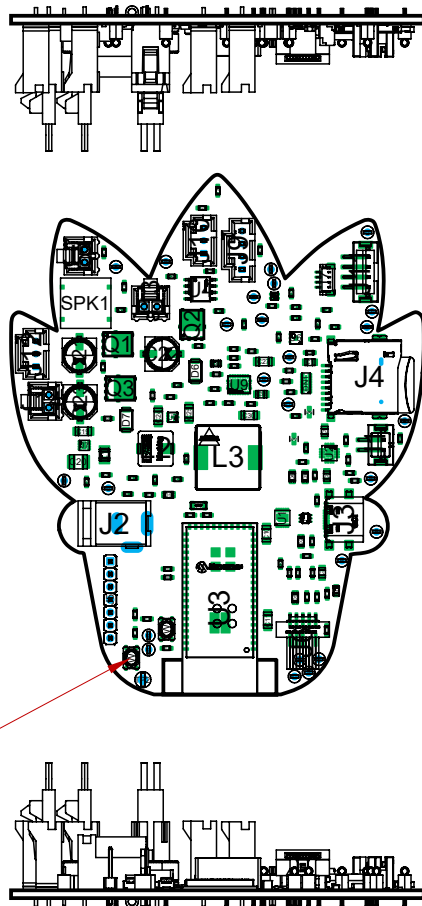
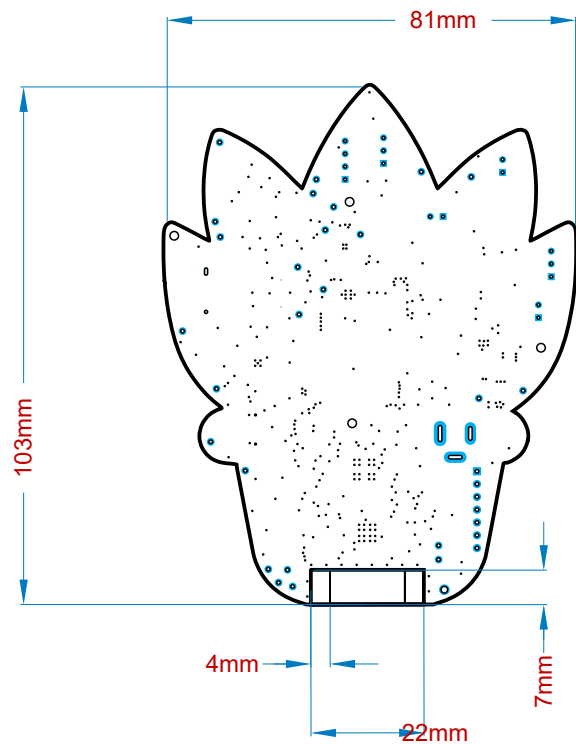
Board Layer Stack Bottom Overlay (Scale 2:1)



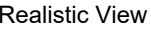
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PCB DOC: =PCB_DWG_NO		SCALE:		FILE NAME: FabricationDrawings.PCBDwf		SHEET: 12		OF 12	

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REV STATUS OF SHEETS	REV											REVISIONS				
	SHEET											ZONE	REV	DESCRIPTION	DATE	APPROVED



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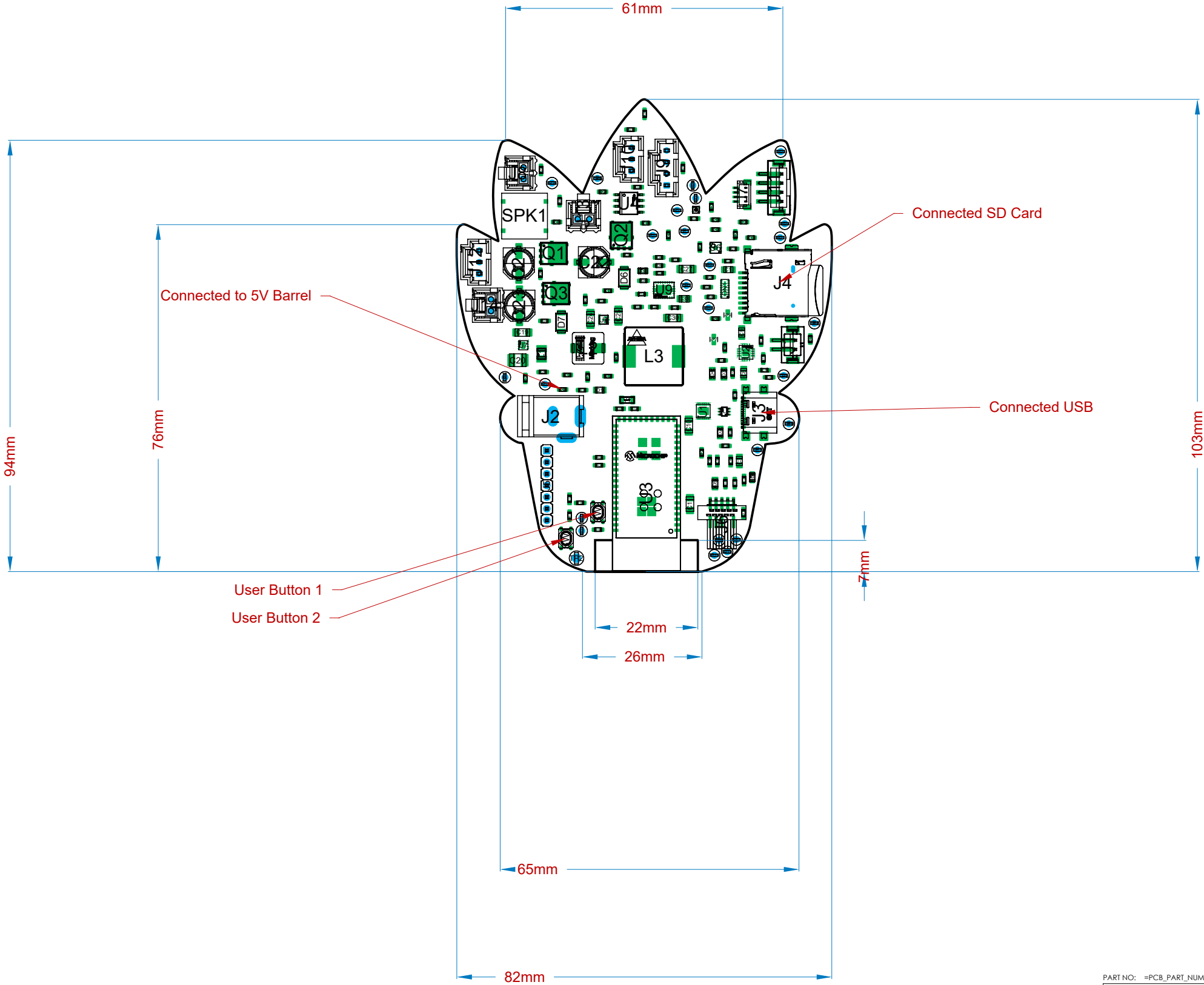
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THIRD ANGLE PROJECTION



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REV STATUS OF SHEETS	REV											REVISIONS					
	SHEET											ZONE	REV	DESCRIPTION	DATE	APPROVED	



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Altium

DESIGN ITEM: SRC-ESE5160 - T13

DESIGN ITEM REVISION: A.4

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SCALE:

FILE NAME: AssemblyDrawings.PCBDwf

SHEET: 3 OF 4

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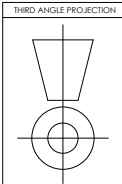
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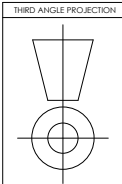
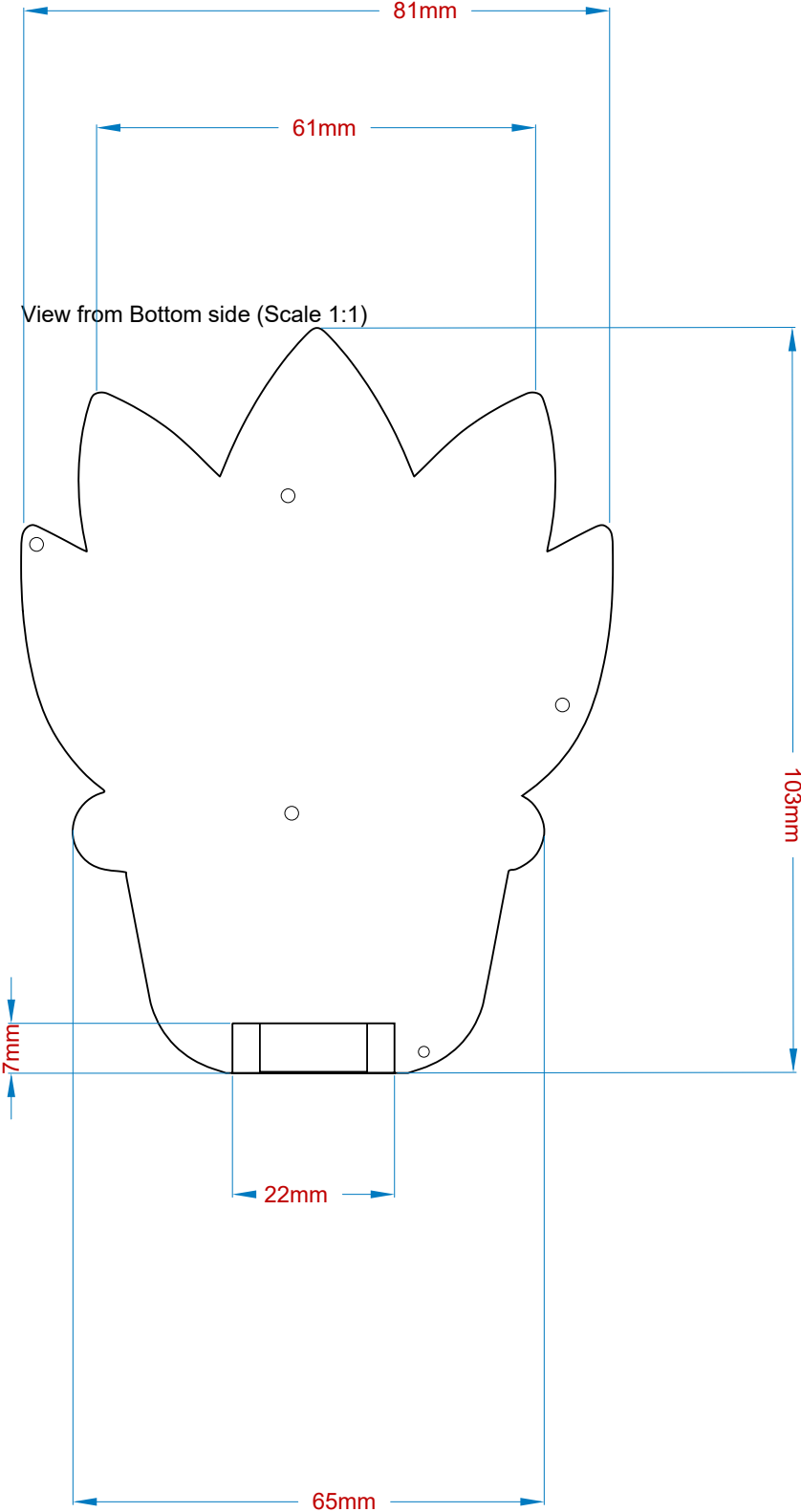
REV:



APPLICATION	
NEXT ASSY	USED ON

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REV STATUS OF SHEETS	REV											REVISIONS				
	SHEET											ZONE	REV	DESCRIPTION	DATE	APPROVED



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CHECKER:	=PCB_CHECKER	=PCB_CHECKER		=PCB_CHECKER				=Address4	
Reference Documents				TITLE:		DESIGN ITEM REVISION: A.4			
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ASSY DOC:		=DOC_NO_FAB_DWG							
SCH DOC:		=DOC_NO_SCH_DWG							
PCB DOC:		=PCB_DWG_NO							
THIRD ANGLE PROJECTION		NEXT ASSY		USED ON		APPLICATION		SHEET: 4 OF 4	